

WHAT IS CLAIMED IS:

- 1 1. A method of compressing puncture mask information comprising:
2 making a delayed puncture mask by:
3 deleting the last k bits of the puncture mask; and
4 appending k zeros to the beginning of the puncture mask;
5 making a differential puncture mask by XORing the delayed puncture
6 mask with the puncture mask; and
7 compressing the differential puncture mask.
- 1 2. The method of claim 1 further comprising:
2 storing the differential puncture mask in a semiconductor memory.
- 1 3. The method of claim 1, wherein compressing the differential
2 puncture mask comprises:
3 starting with the k+1 bit of the puncture mask, counting the number of
4 zeros until a one is reached; and
5 storing the number of zeros in memory.
- 1 4. The method of claim 1 wherein the length of the puncture mask is
2 at least 1000 bits.
- 1 5. The method of claim 1 wherein the length of the puncture mask is
2 at least 2000 bits.
- 1 6. The method of claim 1 wherein puncture masks from at least two
2 communication standards are compressed.
- 1 7. The method of claim 1 wherein at least 30 puncture masks are
2 compressed.
- 1 8. A method of decompressing and using a puncture mask
2 comprising:
3 providing a compressed differential puncture mask;
4 decompressing the compressed differential puncture mask;
5 storing the first k bits of the decompressed differential puncture mask as
6 the first k bits of a decompressed puncture mask;

7 starting with the $k+1$ bit of the decompressed differential puncture mask;
8 XORing the $k+1$ bit of the decompressed differential puncture mask with
9 the 1st bit of the decompressed differential puncture mask resulting in a product; and
10 storing the product as the $k+1$ bit of the decompressed puncture mask.

1 9. The method of claim 8 wherein the length of the decompressed
2 puncture mask is at least 1000 bits.

1 10. The method of claim 8 wherein the length of the decompressed
2 puncture mask is at least 2000 bits.

1 11. The method of claim 8 wherein puncture masks from at least two
2 communication standards are compressed.

1 12. The method of claim 8 wherein at least 30 puncture masks are
2 compressed.

1 13. The method of claim 8 further comprising:
2 continuing with each bit in the decompressed differential puncture mask
3 until the last bit is reached;
4 XORing each $k+i$ bit of the decompressed differential puncture mask with
5 an i bit of the puncture mask resulting in a product; and
6 storing the product as the i bit of the decompressed puncture mask.

1 14. The method of claim 13 further comprising wherein the
2 decompressing of the compressed differential puncture mask is done using run length
3 decoding.

1 15. The method of claim 14 wherein the run length decoding
2 comprises:
3 starting with the $k+1$ bit of the compressed differential puncture mask;
4 creating a decompressed differential puncture mask by writing in series a
5 number of zeros corresponding to a value given by the next L bits of the compressed
6 differential puncture mask; and
7 writing a one to the decompressed differential puncture mask.

1 16. The method of claim 15 wherein the run length decoding further
2 comprises:
3 repeating the starting, creating, and writing, beginning with the $k+1+nL$ bit
4 of the compressed differential puncture mask, wherein n is incremented by one each time,
5 until an end of the compressed differential puncture mask is reached.

1 17. The method of claim 16 further comprising:
2 after the storing the product as the i bit of the puncture mask, using the
3 puncture mask to delete chips from a data sequence, wherein a bit in the puncture mask
4 having a first polarity results in a first corresponding bit in the data sequence being
5 deleted, and a bit in the puncture mask having a second polarity results in a second
6 corresponding bit in the data sequence not being deleted.

1 18. The method of claim 16 further comprising:
2 after the storing the product as the i bit of the puncture mask, reading a
3 data sequence one bit at a time;
4 reading the puncture mask one bit at a time simultaneously with reading
5 the data sequence one bit at a time;
6 inserting an erasure after the previously read data sequence bit if the
7 corresponding puncture mask bit has a first polarity, and not inserting an erasure after the
8 previously read data sequence bit if the corresponding puncture mask bit has a second
9 polarity.

1 19. A code puncture apparatus comprising:
2 a run length decoder having an input and an output;
3 a differential operator having a first input, a second input, and an output,
4 the first input coupled to the output of the run length decoder; and
5 a puncture mask register having a first input, a second input, a first output,
6 and a second output, the second input coupled to the output of the differential operator,
7 and the first output coupled to the second input of the differential operator.

1 20. The apparatus in claim 19 further comprising:
2 a semiconductor memory for storing compressed puncture masks; and

3 a switch coupled to the output of the semiconductor memory and having
4 two positions, wherein a first position is coupled to the input of the run length decoder,
5 and a second position is coupled to the first input of the puncture mask register.

1 21. A method of electronically storing puncture masks comprising:
2 compressing a puncture mask; and
3 storing the compressed puncture mask electronically.

1 22. The method of claim 21 wherein the length of the puncture mask
2 before compression is at least 1000 bits.

1 23. The method of claim 21 wherein the length of the puncture mask
2 before compression is at least 2000 bits.

1 24. The method of claim 21 wherein puncture masks from at least two
2 communication standards are compressed.

1 25. The method of claim 21 wherein at least 30 puncture masks are
2 compressed.

1 26. The method of claim 21 wherein the compressed puncture mask is
2 stored electronically in a semiconductor memory.

1 27. A method of using puncture masks comprising:
2 retrieving a compressed puncture mask from a semiconductor memory;
3 and
4 decompressing the compressed puncture mask.

1 28. The method of claim 27 wherein the length of the decompressed
2 puncture mask is at least 1000 bits.

1 29. The method of claim 27 wherein the length of the decompressed
2 puncture mask is at least 2000 bits.

1 30. The method of claim 27 wherein puncture masks from at least two
2 communication standards are compressed.

1 31. The method of claim 27 wherein at least 30 puncture masks are
2 compressed.

1 32. The method of claim 27 further comprising:
2 using the decompressed puncture mask to delete chips from a data
3 sequence, wherein a bit in the decompressed puncture mask having a first polarity results
4 in a first corresponding bit in the data sequence being deleted, and a bit in the
5 decompressed puncture mask having a second polarity results in a second corresponding
6 bit in the data sequence not being deleted.

1 33. The method of claim 27 further comprising:
2 reading a data sequence one bit at a time;
3 reading the puncture mask one bit at a time simultaneously with reading
4 the data sequence one bit at a time;
5 inserting an erasure after the previously read data sequence bit if the
6 corresponding puncture mask bit has a first polarity, and not inserting an erasure after the
7 previously read data sequence bit if the corresponding puncture mask bit has a second
8 polarity.

1 34. An integrated circuit having a memory wherein the memory
2 comprises a plurality of compressed puncture masks.

1 35. The integrated circuit of claim 34 further comprising circuitry for
2 wireless communications.

1 36. The integrated circuit of claim 34 wherein the length of one of the
2 plurality of puncture masks before compression is at least 1000 bits.

1 37. The integrated circuit of claim 34 wherein the length of one of the
2 plurality of puncture masks before compression is at least 2000 bits.

1 38. The integrated circuit of claim 34 wherein puncture masks from at
2 least two communications standards are compressed.

1 39. The integrated circuit of claim 34 wherein at least 30 puncture
2 masks are compressed.

1 40. The integrated circuit of claim 35 wherein the circuitry for wireless
2 communications comprises at least a portion of a receive path including at least a portion
3 of a mixer.

1 41. The integrated circuit of claim 35 wherein the circuitry for wireless
2 communications comprises at least a portion of a transmit path including at least a portion
3 of a mixer.

1 42. The integrated circuit of claim 41 wherein the portion of the
2 transmit path further comprises at least a portion of a VCO.

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